L Number	Hits	Search Text	DB	Time stamp
19	1	("6551175").PN.	USPAT; US-PGPUB	2004/04/15 14:35
20	117	(polishing or polish) and CMP and ((particle or abrasive) with (size or diameter))	EPO; JPO; DERWENT	2004/04/15 14:48
21	44	((polishing or polish) and CMP and ((particle or abrasive) with (size or diameter))) and nm	EPO; JPO; DERWENT	2004/04/15 15:21
22	1687	(polishing or polish) and CMP and ((particle or abrasive) with (size or diameter))	USPAT; US-PGPUB	2004/04/15 14:49
23	890	((polishing or polish) and CMP and ((particle or abrasive) with (size or diameter))) and nm	USPAT; US-PGPUB	2004/04/15 14:49
24	369	(((polishing or polish) and CMP and ((particle or abrasive) with (size or diameter))) and nm) and ((second or secondary) with (particles or abrasive or grains))	USPAT; US-PGPUB	2004/04/15 14:50
26	1	("6338744").PN.	USPAT; US-PGPUB	2004/04/15 15:22
27	0	korea and "200023851"	EPO; DERWENT	2004/04/15 15:22
28	0	korea and "20002-3851"	EPO; DERWENT	2004/04/15 15:22
29	0	korea and ("20002" with "3851")	EPO; DERWENT	2004/04/15 15:23
30	7	korea and cmp	EPO; DERWENT	2004/04/15 15:23
25	124	((((polishing or polish) and CMP and ((particle or abrasive) with (size or diameter))) and nm) and ((second or secondary) with (particles or abrasive or grains))) and @ad<20000821	USPAT; US-PGPUB	2004/04/15 15:47
31	75	(((((polishing or polish) and CMP and ((particle or abrasive) with (size or diameter))) and nm) and ((second or secondary) with (particles or abrasive or grains))) and @ad<20000821) and copper	USPAT; US-PGPUB	2004/04/15 15:47
32	53	((((((polishing or polish) and CMP and ((particle or abrasive) with (size or diameter))) and nm) and ((second or secondary) with (particles or abrasive or grains))) and @ad<20000821) and copper) and (opening or hole or opening or access or trench or via)	USPAT; US-PGPUB	2004/04/15 15:48
33	28	(((((((polishing or polish) and CMP and ((particle or abrasive) with (size or diameter))) and nm) and ((second or secondary) with (particles or abrasive or grains))) and @ad<20000821) and copper) and (opening or hole or opening or access or trench or via)) and ratio	USPAT; US-PGPUB	2004/04/15 15:48

US-PAT-NO: 6332835

DOCUMENT-IDENTIFIER: US 6332835 B1
See image for Certificate of Correction

TITLE: Polishing apparatus with transfer arm for moving
polished object without drying it

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Detailed Description Text - DETX (17):
Now, let us look into potassium adhesion and the chemical reaction that
takes place as a result of potassium adhesion. Take, for example, the reaction
of cation exchange resin. It essentially consists in neutralization as shown
in FIG. 3. Assume now that silicon oxide does not satisfy the stoichiometric
atomic **ratio**. Then, potassium will presumably adhere to nonstoichiometric
silicon oxide by way of the reactions shown in FIG. 3.

Detailed Description Text - DETX (27):
Objects apt to be adhered by potassium includes compound insulators formed
by deposition by means of plasma CVD at temperature below 800.degree. C. and,
if necessary, heat treated at temperature between 100.degree. C. and
450.degree. C. and those formed by deposition by means of sputtering and, if
necessary, heat treated. Oxide insulators formed by a plasma treatment of
exposing the substrate surface to oxygen plasma and, if necessary, heat treated
are also apt to be adhered by potassium. Even insulators carrying silicon
oxide film produced by thermal oxidation are apt to be adhered by potassium if
the surface is at least partly subjected to a subsequent plasma treatment such

as plasma etching. Such insulators are absolutely required to be polished if
they are to be used as interlayer insulation film in a multilayer wired
section. Specific insulators include noncrystalline compounds such as silicon
oxide, silicon nitride, or silicon nitride oxide, which may be, if necessary,
doped with boron, phosphor or fluorine. The compound film layer formed by any
of the above plasma treatment techniques mostly contains a noncrystalline
compound having a nonstoichiometric atomic **ratio** that is not compatible with
the stoichiometric atomic **ratio**. Film formed by deposition by means of thermal
CVD or photo-excited CVD is also apt to adsorb potassium.

Detailed Description Text - DETX (29):

A preferable polishing agent to be used for the purpose of the invention
contains **particles** of silica (SiO.sub.2), alumina (Al.sub.2 O.sub.3) and/or
cerium oxide (CeO) having a primary **particle diameter** between about 1 and 300
nm and a secondary particle diameter between about 3 and 1,000 **nm** and dispersed
in a dispersant, which is preferably an aqueous solution that contains
potassium typically in the form of KOH, K.sub.3 Fe(CN).sub.6 or potassium
acetate.

Detailed Description Text - DETX (56):

A silicon oxide film 102 having a nonstoichiometric compositional **ratio** is
formed to a thickness between 1.5 and 2.5 microns by a plasma CVD technique,
using tetraethoxysilane (TEOS), on the silicon wafer 100 having the lower wired
layer 101 (Step S2, FIG. 12B).

Detailed Description Text - DETX (57):

Then, the silicon oxide film is polished by about 500 **nm** to 1.2 .mu.m by

means of a polishing apparatus as shown in FIGS. 8 and 9, a polishing agent
prepared by dispersing fine particles of silica with a **particle diameter**
between 30 and 250 microns into a KOH-containing aqueous solution and a
polyurethane polishing pad. Thereafter, the polished surface is cleaned by
means of a brush and pure water fed to it within the polishing apparatus.
Subsequently, the wafer is driven to rotate and subjected to a spin cleaning
operation by applying ultra pure water heated to 80.degree. C. and imparted
with ultrasonic vibration with a frequency of 0.95 MHz to the polished surface.
Then, the wafer is dried in a drying chamber before moved out of the polishing
apparatus (Step S3, FIG. 12C).

Detailed Description Text - DETX (61):

Thereafter, the wafer is subjected to a plasma cleaning process in a plasma
cleaning chamber of a cluster type multi-chamber system. Then a Ti/TiN barrier
layer 104 (laminate of a Ti layer and a TiN layer) is formed to a thickness of
20 to 60 **nm** in the sputtering chamber and an aluminum film 105 containing or
not containing copper is formed on the Ti/TiN barrier layer 104 in the aluminum
chamber. Subsequently, a reflow operation is conducted at 400 to 500.degree.
C. (Step S5, FIG. 12E).

Detailed Description Text - DETX (62):

Then, the barrier layer 104 and the aluminum film 105 on the silicon oxide
film 102 are removed by means of CMP, using a slurry obtained by dispersing
fine particles of silica into water or solutions, to which ammonium iron
sulfate is added by 0.01 to 0.5 mol/liter, until the barrier layer 104 and the
aluminum film 105 are left only in the contact holes (Step S6, FIG. 12F).

After cleansing the surface, a TiN layer 106 is formed to a thickness of 20 to 60 **nm** by sputtering and then an aluminum silicon film 107 is formed to a thickness of 1 to 2 microns also by sputtering, which films are then etched to produce a wiring pattern. Then, silicon oxide film 108 is formed to a thickness of about 2 microns by plasma CVD. The silicon oxide film shows undulations to reflect the wiring pattern (Step S7, FIG. 12G). The above steps will be repeated when a multiple of wiring layers are to be produced.

Detailed Description Text - DETX (65):

A silicon oxide film 102 having a nonstoichiometric compositional **ratio** is formed by a plasma CVD technique or some other techniques, using tetraethoxysilane (TEOS), on the silicon wafer 100 having the lower wired layer 101 (Step S2, FIG. 13B).

Detailed Description Text - DETX (66):

Then, the silicon oxide film is polished by about 500 **nm** to 1.2 .mu.m by means of a polishing apparatus as shown in FIGS. 8 and 9, a polishing agent prepared by dispersing fine particles of silica with a **particle diameter** between 30 and 250 microns into a KOH-containing aqueous solution and a polyurethane polishing pad. Thereafter, the polished surface is cleaned by means of a brush and pure water fed to it within the polishing apparatus. Subsequently, the wafer is driven to rotate and subjected to a spin cleaning operation by applying ultra pure water heated to 80.degree. C. and imparted with ultrasonic vibration with a frequency of 0.95 MHz to the polished surface. Then, the wafer is dried in a drying chamber before moved out of the polishing apparatus. A silicon nitride film is formed by plasma CVD

and subsequently a
silicon oxide film 102 is formed once again by plasma CVD (Step S3, FIG. 13C).

Detailed Description Text - DETX (68):
Then, once again, hexamethyldisilazane (HMDS) is applied to the wafer and
subsequently photoresist is applied thereto to a film thickness between 1.0 and
1.3 microns. Then, the wafer is baked. The baked wafer is then put into an
aligner and exposed to light to form a latent image of a pattern to be used for
producing a contact hole. The wafer is removed from the aligner and the latent
image of the photoresist is developed. Subsequently, the wafer is put into a
reactive ion etching system in order to anisotropically etch the silicon
nitride film and the exposed silicon oxide and produce a patterned contact
hole, using the developed photoresist pattern as mask (Step S4, FIG. 13D). The
etch selectivity **ratio** of silicon oxide and silicon nitride can be modified by
modifying, for example, the **ratio** of the flow rate of CF.sub.4 to that of
CHF.sub.3.

Detailed Description Text - DETX (72):
Thereafter, the wafer is subjected to a plasma cleaning process in the
plasma cleaning chamber of a cluster type multi-chamber system. Then a Ti/TiN
barrier layer 104 (laminate of a Ti layer and a TiN layer) is formed to a
thickness of 20 to 60 **nm** in the sputtering chamber and an aluminum film 105
containing or not containing copper is formed on the Ti/TiN barrier layer 104
in the aluminum sputtering chamber. Subsequently, a reflow operation is
conducted at 400 to 500.degree. C. (Step S5, FIG. 13E). In place of the
aluminum film, a copper film or a metal film containing copper as principal

ingredient may be formed by CVD, sputtering or plating.

Detailed Description Text - DETX (73):

Then, the barrier layer 104 and the aluminum film 105 on the silicon oxide film 102 are removed by means of CMP, using a slurry obtained by dispersing fine particles of silica into water, to which potassium acetate is added, until the barrier layer 104 and the aluminum film 105 are left only in the groove 113 and the contact holes (Step S6, FIG. 13F). Subsequently, the wafer is cleaned by means of brush and hot pure water to remove fine particles of silica and potassium. After cleansing the surface, a TiN layer 106 is formed to a thickness of 20 to 60 **nm** by sputtering and then heat treated. Thereafter, the film is etched to produce a wiring pattern. Then, silicon oxide film 108 is formed to a thickness of about 2 microns by plasma CVD (Step S7, FIG. 13G). Steps S2 through S7 will be repeated when a multiple of wiring layers are to be produced.

Detailed Description Text - DETX (75):

A total of four monocrystal silicon wafers were prepared and a silicon oxide film having a nonstoichiometric compositional **ratio** is formed by a plasma CVD technique, using TEOS, on each of the wafers.